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Date: August 25, 2006	Pages: 8 (including this sheet)
From: Andrew C. Graham	Sender's Phone No.: (512) 338-6300 Sender's Fax No.: (512) 338-6301

REGARDING:

Title:	INTEGRATED CIRCUIT INCORPORATING THREE-DIMENSIONAL MEMORY ARRAY WITH DUAL OPPOSING DECODER ARRANGEMENT		
Application No.: 10/774,818	Filed:	February 9, 2004	
Examiner: Thong Q. Le	Group Art Unit:	2827	
Atty. Docket No.: 023-0025	Confirmation No.:	9232	

ATTACHED HERETO:

- (1) Response After Final Rejection (37 CFR § 1.116) (7 pages)

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Mark G. Johnson, et al.

Title: Integrated Circuit Incorporating Three-Dimensional Memory Array with
Dual Opposing Decoder Arrangement

Application No.: 10/774,818

Filed: February 9, 2004

Examiner: Thong Quoc Le

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Atty. Docket No.: 023-0025

Confirmation No.: 9232

August 25, 2006

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450**RESPONSE AFTER FINAL REJECTION (37 C.F.R. § 1.116)**

This paper is being submitted following the Final Rejection mailed on May 25, 2006. In light of the Remarks herein, further consideration is requested.

No fee is believed due with this response. However, the Office is authorized to charge Deposit Account 50-0631 for any fee determined to be required by this paper.